

The diagram illustrates a search data setting section (7) with a grid of logic blocks (1a, 1b, 1c, 1d). The inputs to these blocks are labeled 5a, 5b, 5c, and 5d. The outputs are labeled 4a, 4b, 4c, and 4d. The diagram also shows a set of comparators (2, 3) and a bus system (6, 8, 9). The inputs are labeled <1:0>, <3:2>, and <n+1,n>. The output is labeled <bit>.

FIG.2

<n+1,n>

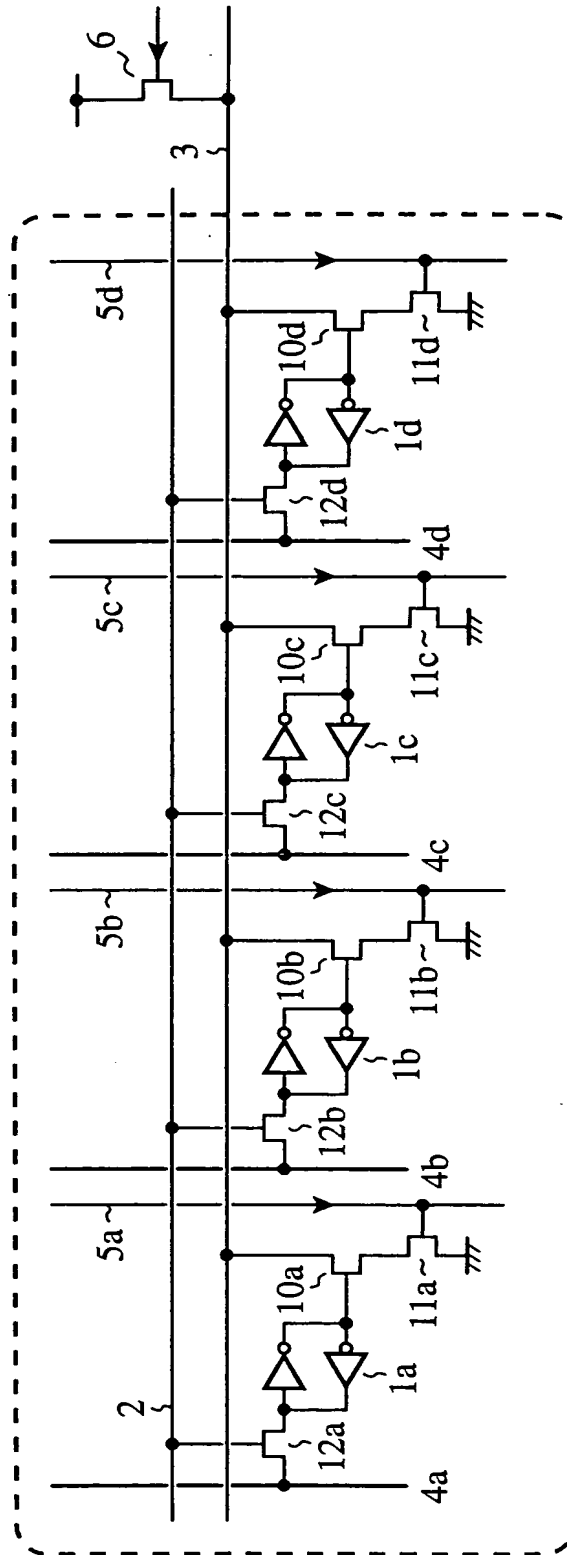


FIG.3

	SEARCH "00" 5a=1,5b=0,5c=0,5d=0	SEARCH "01" 5a=0,5b=1,5c=0,5d=0	SEARCH "10" 5a=0,5b=0,5c=1,5d=0	SEARCH "11" 5a=0,5b=0,5c=0,5d=1
STORE "xx" 1a=0,1b=0,1c=0,1d=0				
STORE "x0" 1a=0,1b=1,1c=0,1d=1		DISCHARGE		DISCHARGE
STORE "x1" 1a=1,1b=0,1c=1,1d=0	DISCHARGE		DISCHARGE	
STORE "0x" 1a=0,1b=0,1c=1,1d=1			DISCHARGE	DISCHARGE
STORE "00" 1a=0,1b=1,1c=1,1d=1		DISCHARGE	DISCHARGE	DISCHARGE
STORE "01" 1a=1,1b=0,1c=1,1d=1	DISCHARGE		DISCHARGE	DISCHARGE
STORE "1x" 1a=1,1b=1,1c=0,1d=0	DISCHARGE	DISCHARGE		
STORE "10" 1a=1,1b=1,1c=0,1d=1	DISCHARGE	DISCHARGE		DISCHARGE
STORE "11" 1a=1,1b=1,1c=1,1d=0	DISCHARGE	DISCHARGE	DISCHARGE	

FIG.4

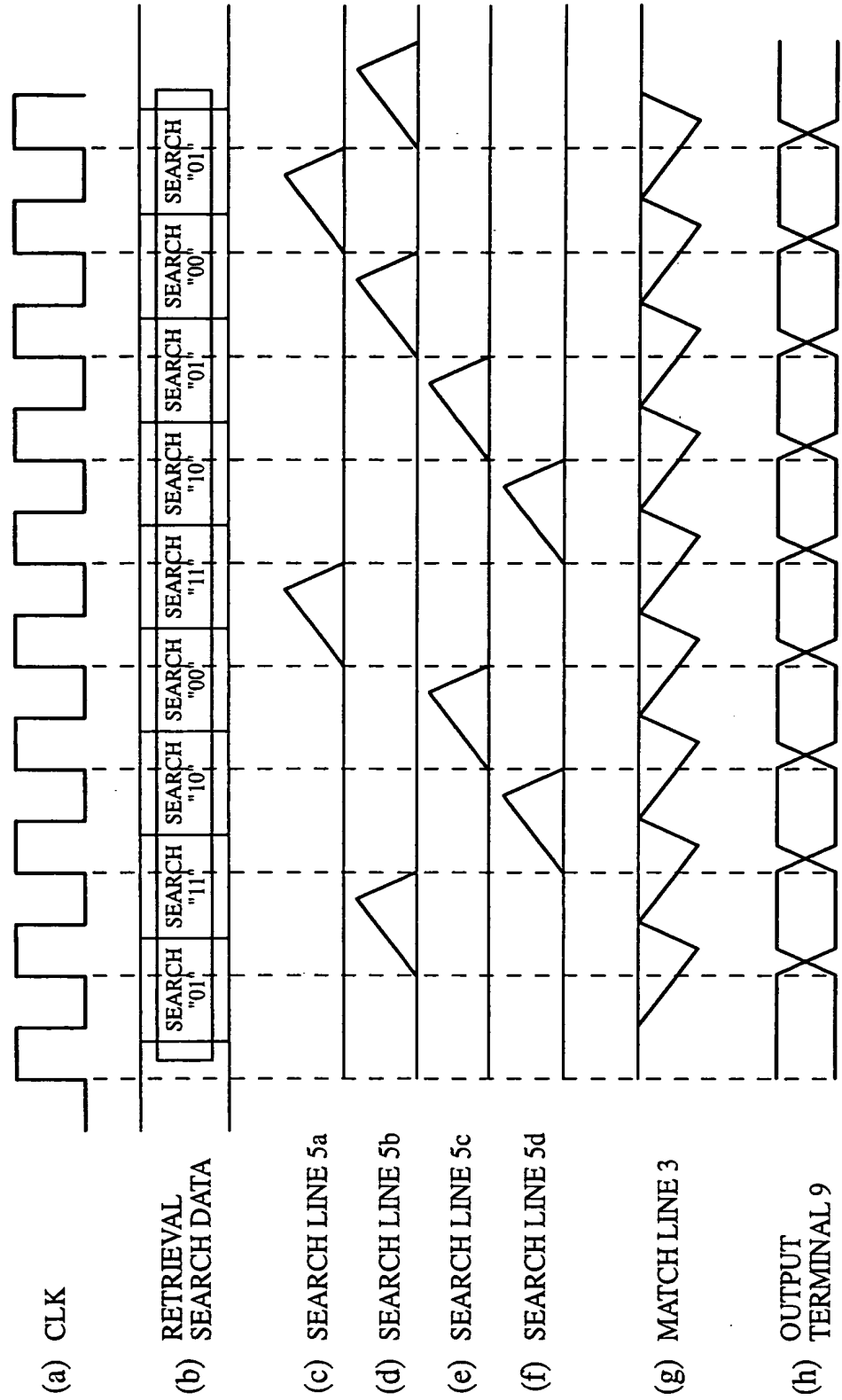


FIG.5

<n+1,n>

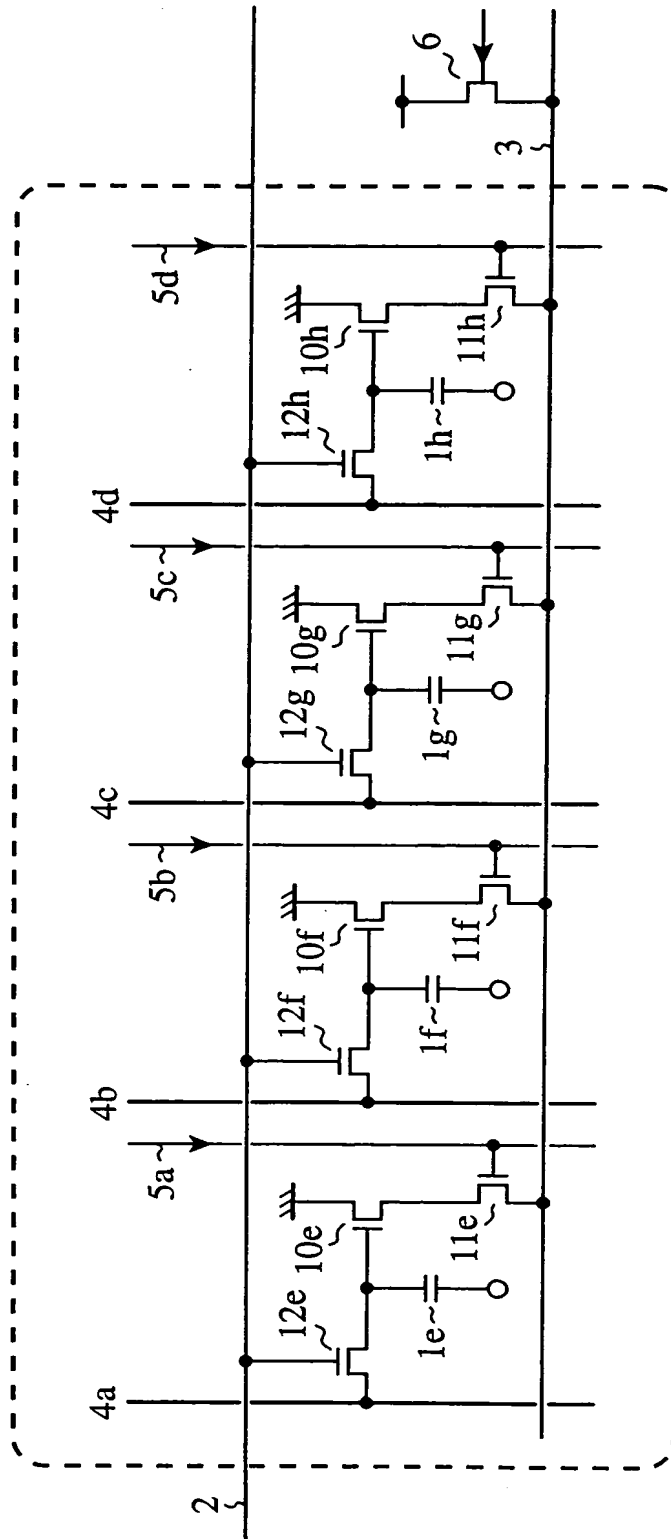


FIG. 6

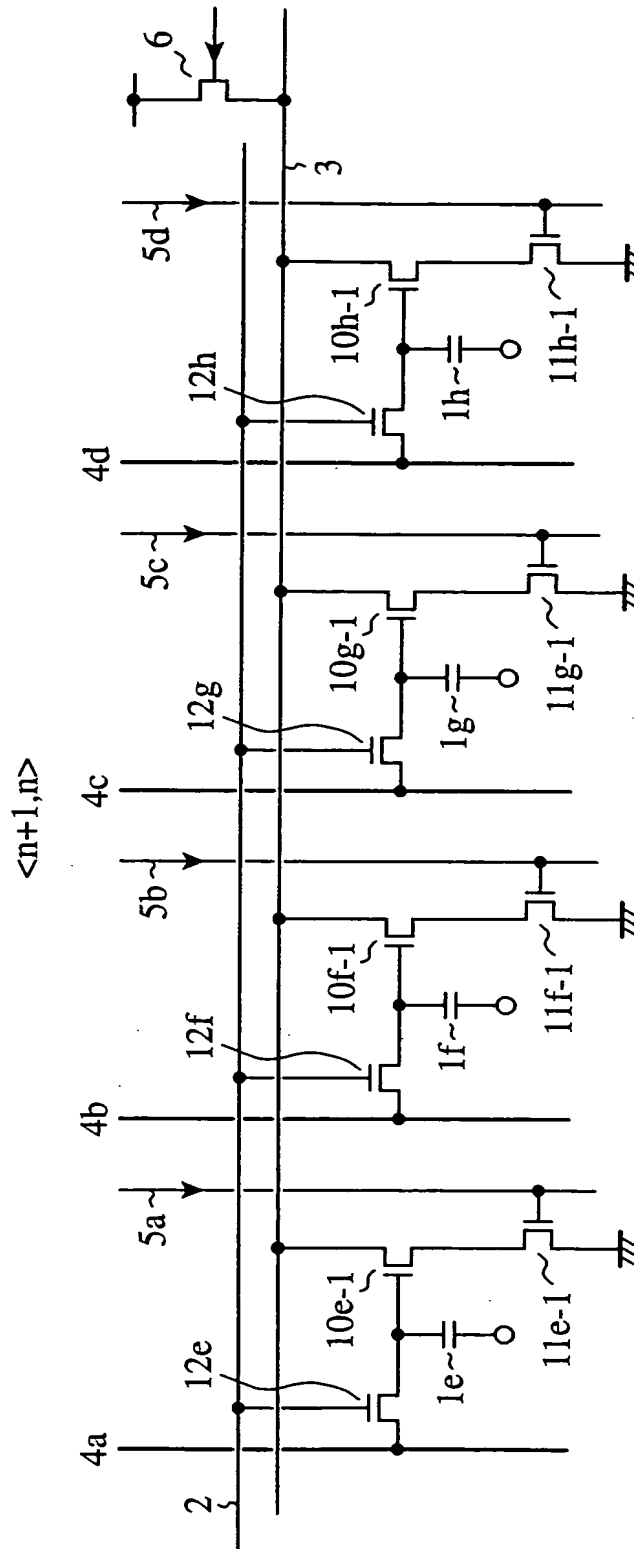


FIG.7B

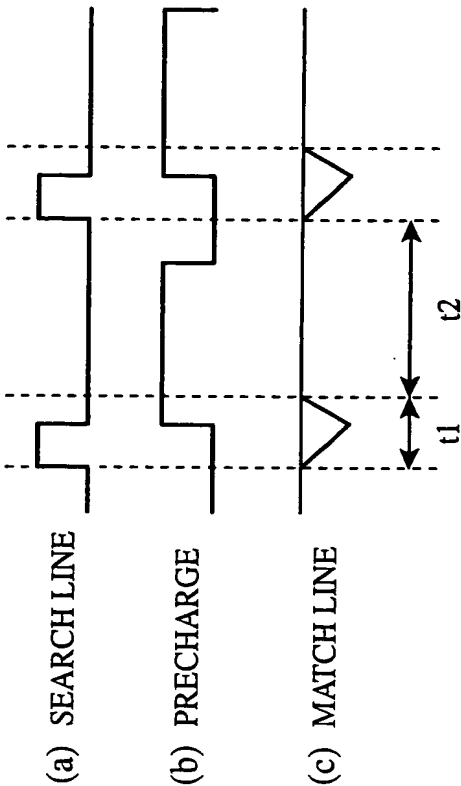


FIG.7A

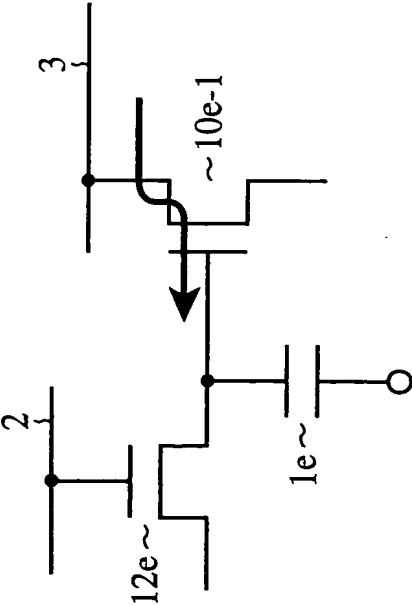


FIG. 8

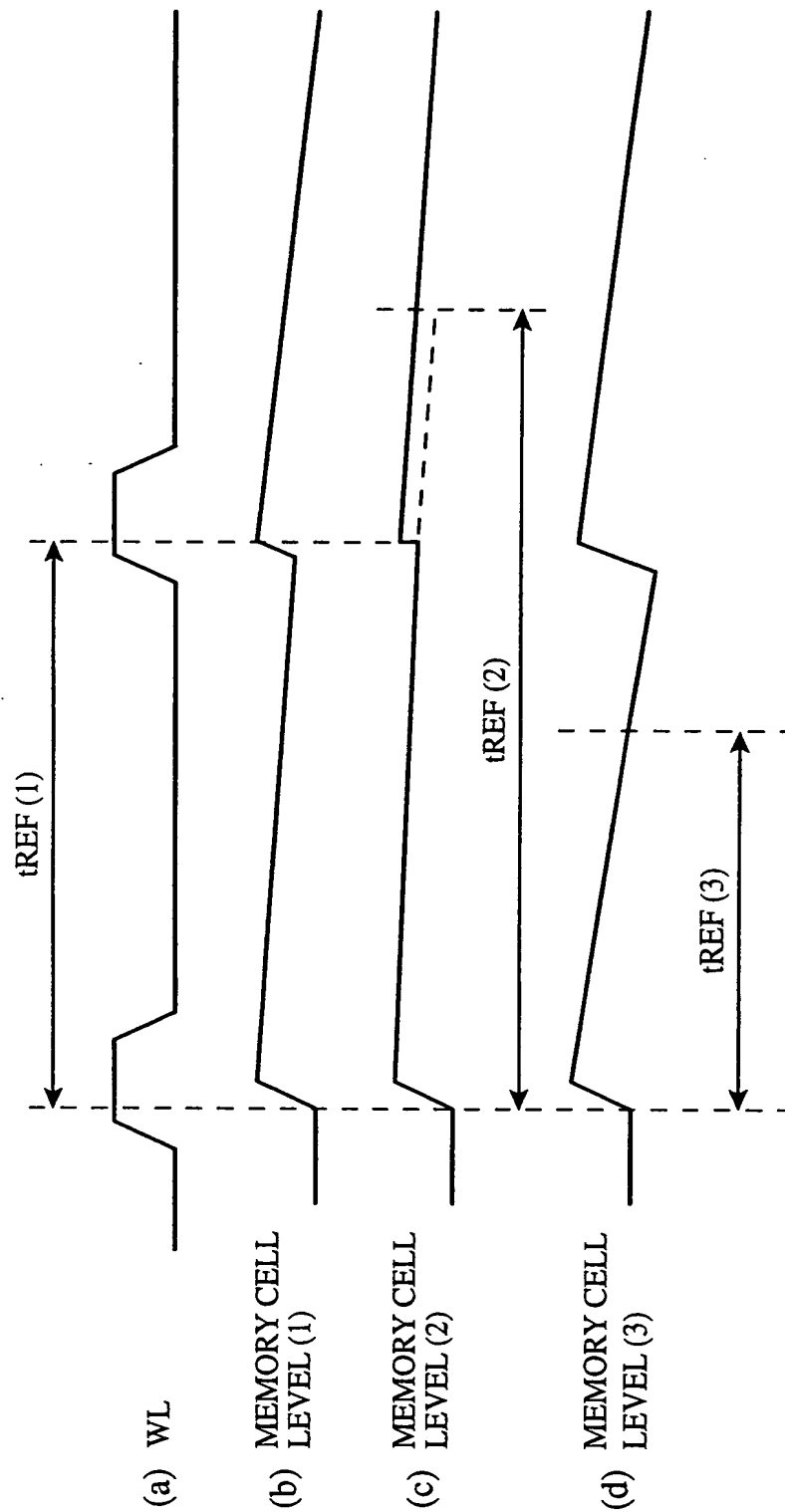


FIG. 9 (PRIOR ART)

